We Claim:

1. A method for fabricating a storage capacitor having a vertical structure with respect to a main surface of a substrate, the method which comprises:

forming a lower, metallic capacitor electrode, a storage dielectric and an upper capacitor electrode in or on the main surface of the substrate; and

performing the step of forming the lower, metallic capacitor electrode in a self-aligned manner on a silicon base material by producing uncovered silicon regions at locations where the lower capacitor electrode will be formed, and then selectively depositing metal silicide from a vapor phase on the uncovered silicon regions.

- 2. The method according to claim 1, wherein the step of producing the uncovered silicon regions includes applying a covering material to the silicon base material.
- 3. The method according to claim 2, which further comprises selecting the covering material from a group consisting of silicon nitride, silicon dioxide, and a combination silicon nitride and silicon dioxide.
- 4. A method for fabricating a memory cell, which comprises:

etching a trench into a main surface of a silicon substrate;

performing the method for fabricating the storage capacitor according to claim 2 such that the storage capacitor is at least partially configured in the trench and the lower metallic capacitor electrode adjoins a wall of the trench;

forming a selection transistor having a source electrode, a drain electrode, a conductive channel and a gate electrode; and

electrically conductively connecting the upper capacitor electrode of the storage capacitor to the source electrode or the drain electrode of the selection transistor.

- 5. The method according to claim 4, wherein the silicon substrate is silicon substrate configured on an insulator.
- 6. A method for fabricating a trench capacitor, which comprises:

etching a trench into a main surface of a semiconductor substrate; and

performing the method for fabricating the storage capacitor according to claim 1 such that the storage capacitor is at least partially configured in the trench and the lower, metallic capacitor electrode adjoins a wall of the trench.

- 7. The method according to claim 1, which further comprises using a metal selected from a group consisting of tungsten, titanium, molybdenum, tantalum, cobalt, nickel, niobium, platinum, palladium and rare earths to form the metal silicide.
- 8. The method according to claim 1, which further comprises after performing the step of producing the uncovered silicon regions, performing a step for increasing a surface area of the uncovered silicon regions.
- 9. A method for fabricating a stacked capacitor, which comprises:

applying a pattern of a polysilicon layer cell to a nonsilicon material;

performing the method for fabricating the storage capacitor according to claim 1; and

selecting the polysilicon layer for use as an electrically conductive connecting structure between the lower, metallic capacitor electrode and a source electrode or a drain electrode of a selection transistor of a DRAM memory cell.

- 10. The method according to claim 1, wherein the step of producing the uncovered silicon regions includes applying a pattern of a silicon layer or a polysilicon layer to a non-silicon material.
- 11. A method for fabricating a memory cell, which comprises:

forming a selection transistor having a source electrode, a drain electrode, a conductive channel and a gate electrode on a main surface of a semiconductor substrate; and

performing the method according to claim 8 such that the lower, metallic capacitor electrode is formed on a surface of an electrically conductive connecting structure made from polysilicon and connecting the lower, metallic capacitor electrode to the source electrode or the drain electrode of the selection transistor.

12. A method for fabricating a trench capacitor, which comprises:

etching a trench into a main surface of a silicon substrate;

producing covered silicon regions by applying a covering material to regions of the trench on which a lower, metallic capacitor electrode should not be formed;

forming the lower, metallic capacitor electrode in a selfaligned manner by selectively forming a metal silicide on
uncovered silicon regions such that the capacitor is at least
partially configured in the trench and the lower, metallic
capacitor electrode adjoins a wall of the trench; and

after forming the lower, metallic capacitor electrode, providing a storage dielectric and an upper capacitor electrode.

- 13. The method according to claim 12, which further comprises selecting the covering material from a group consisting of silicon nitride, silicon dioxide, and a combination of silicon nitride and silicon dioxide.
- 14. A method for fabricating a memory cell, which comprises:

performing the method for fabricating the trench capacitor according to claim 12;

forming a selection transistor having a source electrode, a drain electrode, a conductive channel and a gate electrode; and

electrically conductively connecting the upper capacitor electrode to the source electrode or the drain electrode the selection transistor.

- 15. The method according to claim 14, wherein the silicon substrate is a silicon substrate configured on an insulator.
- 16. The method according to claim 12, wherein the step of selectively forming the metal silicide on the uncovered silicon regions includes:

depositing a metal being suitable for forming a metal-silicon compound with uncovered silicon in a subsequent heat treatment step;

performing a heat treatment at a predetermined temperature in a predetermined atmosphere; and

selectively removing the metal that was not converted into silicide.

- 17. The method according to claim 14, wherein the heat treatment step is carried out at a temperature of 600 to 1000° C in a nitrogen atmosphere.
- 18. The method according to claim 14, wherein the heat treatment step is performed for a duration such that only a part of the metal facing the uncovered silicon forms a metal-silicon compound.